

PARAMETRIC TESTING FOR HIGH PIN COUNT ASIC

Abstract of the Disclosure

A method for reducing Pin Count Test design and test that allows parametric test patterns for high pin count ASICs to be applied using low pin count testers. The same boundary scan structure used to isolate the test of internal logic to a small number of test I/O is also used to apply parametric external I/O tests to the ASIC's functional I/O. The parametric tests are banked into pin groups and applied on the same low pin count tester used for the internal logic tests.

Figures